AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) An integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

memory, including one or more memory arrays for storing information related to the transceiver in predefined memory mapped locations of the memory, the stored information including digital values corresponding to current operating conditions of the optoelectronic transceiver, where said digital values include a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver;

analog to digital conversion circuitry for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic transceiver, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one of said predefined memory mapped locations in the memory;

an interface configured to enable a host to read from host-specified locations within the memory, including said predefined memory mapped locations of the memory, so as to obtain one or more of said digital values corresponding to current operating conditions of the optoelectronic transceiver;

comparison logic configured to compare the at least one digital value with a limit value to generate a flag value; and

operation disable circuitry configured to disable operation of at least part of the optoelectronic transceiver in response to a signal, wherein the signal is based on said flag value.

2. (Previously Presented) The integrated circuit of claim 1, wherein the operation disable circuitry is configured to disable operation of the optoelectronic transceiver in response to a signal sent to a disable pin in the optoelectronic transceiver.

3. (Previously Presented) The integrated circuit of claim 1, wherein the limit value is dependent on a temperature of the optoelectronic transceiver.

4. (Currently Amended) An integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

memory, including one or more memory arrays for storing information related to the transceiver in predefined memory mapped locations of the memory, the stored information including digital values corresponding to current operating conditions of the optoelectronic transceiver, where said digital values include a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver;

analog to digital conversion circuitry for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic transceiver, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one of said predefined memory mapped locations in the memory;

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory;

an interface configured to enable a host to read from host specified locations within the memory, including said predefined memory mapped locations of the memory, so as to obtain one or more of said digital values corresponding to current operating conditions of the optoelectronic; and

comparison logic configured to compare the at least one digital value with a limit value to generate a flag value;

wherein the control circuitry includes operation disable circuitry configured to disable operation of at least part of the optoelectronic transceiver in response to a disable signal generated by the control circuitry based on the flag value.

5. (Previously Presented) The integrated circuit of claim 4, wherein the operation disable circuitry is configured to disable operation of the optoelectronic transceiver in response to a signal sent to a disable pin in the optoelectronic transceiver.

6. (Previously Presented) The integrated circuit of claim 4, wherein the limit value is dependent on a temperature of the optoelectronic transceiver.

7. (Previously Presented) The integrated circuit of claim 4, further comprising a temperature look up table used in generating control signals based on a temperature of the optoelectronic transceiver.

8. (Currently Amended) An integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

memory, including one or more memory arrays for storing information related to the transceiver in predefined memory mapped locations of the memory, the stored information including digital values corresponding to current operating conditions of the optoelectronic transceiver, where said digital values include a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver;

analog to digital conversion circuitry for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic transceiver, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one of said predefined memory mapped locations in the memory;

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory;

an interface for allowing a host to read from host specified locations within the memory, including said predefined memory mapped locations of the memory, so as to obtain one or more of said digital values corresponding to current operating conditions of the optoelectronic transceiver; and

wherein the control circuitry includes circuitry configured to adjust one or more control signals in accordance with an adjustment value stored in the memory by the host via said interface.

9. (Previously Presented) The integrated circuit of claim 8, wherein the adjustment value corresponds to a deviation from a configured operating condition of the optoelectronic transceiver.

10. (Previously Presented) The integrated circuit of claim 8, wherein the control circuitry is configured to adjust the one or more control signals by scaling the control signals.

11. (Previously Presented) The integrated circuit of claim 8, wherein the control circuitry is configured to adjust the one or more control signals by an amount specified by the adjustment value.

12. (Currently Amended) A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

in accordance with instructions received from a host device, enabling the host device to read from and write to host specified locations within a controller of the optoelectronic transceiver, the host specified locations including a set of predefined memory mapped locations in which are stored digital values corresponding to current operating conditions of the optoelectronic transceiver, said stored digital values including a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver;

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in the controller, the converted digital values including said digital values corresponding to current operating conditions of the optoelectronic transceiver; and

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in predefined memory mapped locations within the controller; and

testing operation of the device at a known deviation from a configured operating condition of the optoelectronic transceiver by adjusting one or more control signals in accordance with an adjustment value stored in the controller.

13. (Original) The method of claim 12, wherein the adjusting includes scaling the control signals by the adjustment value.

14. (Currently Amended) A circuit for an optoelectronic transceiver, which includes a laser transmitter and a photodiode receiver, said circuit comprising:

analog to digital conversion circuitry configured to convert analog signals

corresponding to operating conditions of said optoelectronic transceiver into digital values;

memory configured to store said digital values in predefined memory mapped locations, where said digital values stored in said predefined memory mapped locations include: a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver; and

an interface configured to enable a host to read from said predefined memory mapped locations in memory.

15. (Currently Amended) The circuit of claim 14, wherein each of said predefined memory mapped locations are associated with a unique address in said memory.

16. (Previously Presented The circuit of claim 14, wherein each of said digital values is a 16 bit number.

17. (Previously Presented) The circuit of claim 14, further comprising a temperature sensor for measuring said temperature of said optoelectronic transceiver.

18. (Previously Presented) The circuit of claim 14, further comprising a supply voltage sensor for measuring said supply voltage of said optoelectronic transceiver.

19. (Currently Amended) The circuit of claim 14, wherein said interface is also configured to enable said host to read from and write to host-specified memory mapped addresses within the memory.

20. (Previously Presented) The circuit of claim 14, further comprising comparison logic configured to compare at least one of said digital values with a limit value to generate a flag value.

21. (Previously Presented) The circuit of claim 20, further comprising operation disable circuitry configured to disable operation of at least part of the optoelectronic transceiver in response to a signal based on said flag value.

22. (Previously Presented) The circuit of claim 21, wherein the operation disable circuitry is configured to disable operation of the optoelectronic transceiver in response to a signal sent to a disable pin in the optoelectronic transceiver.

23. (Previously Presented) The circuit of claim 20, wherein the limit value is dependent on said temperature of said optoelectronic transceiver.

24. (Previously Presented) The circuit of claim 14, further comprising control circuitry configured to generate control signals to control operation of said laser transmitter in accordance with one or more values stored in memory.

25. (Previously Presented) The circuit of claim 24, wherein said control circuitry includes operation disable circuitry configured to disable operation of at least part of said optoelectronic transceiver.

26. (Previously Presented) The circuit of claim 14, wherein said memory further comprises one or more memory arrays for storing information related to said optoelectronic transceiver.

27. (Previously Presented) The circuit of claim 14, wherein a portion of said memory is reserved for optional warning flags.

28. (Previously Presented) The circuit of claim 27, wherein said optional warning flags are selected from a group consisting of: a temperature high warning, a temperature low warning, a high supply voltage warning, a low supply voltage warning, a high laser bias current warning, a low laser bias current warning, a high output power warning, a low output power warning, a high received optical power warning, and a low received optical power warning.

29. (Previously Presented) The circuit of claim 14, wherein a portion of said memory is reserved for optional alarm flags.

30. (Previously Presented) The circuit of claim 29, wherein said optional alarm flags are selected from a group consisting of: a temperature high alarm, a temperature low alarm, a high supply voltage alarm, a low supply voltage alarm, a high laser bias current alarm, a low

laser bias current alarm, a high output power alarm, a low output power alarm, a high received optical power alarm, and a low received optical power alarm.

31. (Previously Presented) The circuit of claim 14, wherein a portion of said memory is reserved for an optional indication of a state of a transmitter disable input pin.

32. (Previously Presented) The circuit of claim 14, wherein a portion of said memory is reserved for an optional indication of a state of a software disable.

33. (Previously Presented) The circuit of claim 14, wherein a portion of said memory is reserved for a password that controls access to said memory.

34. (Currently Amended) A circuit for an optoelectronic transceiver, comprising:

analog to digital conversion circuitry configured to convert analog signals corresponding to operating conditions of an optoelectronic transceiver into 16 bit digital values;

memory configured to store said digital values in predefined memory mapped locations identified by unique addresses, where said digital values comprise: a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of a laser transmitter of said optoelectronic transceiver, an output power of said laser transmitter, and a received optical power of a photodiode receiver of said optoelectronic transceiver; and

an interface configured to enable a host having ~~at least one of~~ said addresses to read said digital values from ~~at least one of~~ said predefined memory mapped locations in memory.

35. (Previously Presented) The circuit of claim 34, further comprising:

a temperature sensor for measuring said temperature of said optoelectronic transceiver; and

a supply voltage sensor for measuring said internal supply voltage of said optoelectronic transceiver.

36. (Previously Presented) The circuit of claim 34, wherein said interface is also configured to enable said host to read from and write to host-specified memory-mapped locations within the memory.

37. (Previously Presented) The circuit of claim 34, wherein a portion of said memory is reserved for information selected from a group consisting of: optional warning flags, optional alarm flags, an optional indication of a state of a transmitter disable input pin, an optional indication of a state of a software disable feature of said optoelectronic transceiver, and a password that controls access to said memory.

38. (Currently Amended) An optoelectronic transceiver, comprising:

a housing;

a laser transmitter at least partially contained within said housing;

a photodiode receiver at least partially contained within said housing;

circuitry at least partially contained, said circuitry comprising:

analog to digital conversion circuitry configured to convert analog signals corresponding to operating conditions of an optoelectronic transceiver into digital values;

memory configured to store said digital values in predefined memory mapped locations identified by unique addresses, where said digital values comprise: a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver; and

an interface configured to enable a host having ~~at least one of~~ said addresses to read said digital values from ~~at least one of~~ said predefined memory mapped locations in memory.